IN THE CLAIMS

Claims 1-17 (cancelled).

18. (Original) An integrated circuit comprising:

a semiconductor substrate;

a dielectric ("select gate dielectric") on the semiconductor substrate;

a select gate of a nonvolatile memory cell on the select gate dielectric;

a floating gate of the nonvolatile memory cell;

a control gate of the nonvolatile memory cell, a portion of the control gate overlying the select gate;

a first peripheral transistor for accessing the memory cell, the first peripheral transistor comprising:

a first peripheral transistor gate dielectric on the semiconductor substrate; and

a gate on the first peripheral transistor gate dielectric;

wherein the first peripheral transistor gate dielectric has the same thickness as the select gate dielectric.

19. (Original) The integrated circuit of Claim 18 wherein the semiconductor substrate comprises a channel region of the memory cell, wherein the select gate controls a conductivity of a portion of the channel region, and the floating gate overlies another portion of the channel region.

20. (Original) The integrated circuit of Claim 19 wherein the control gate overlies the floating gate.

21. (Original) The integrated circuit of Claim 18 wherein the semiconductor substrate is a silicon substrate, and the select gate dielectric and the first peripheral transistor gate dielectric consist of silicon oxide.

22. (Original) The integrated circuit of Claim 18 further comprising a dielectric ("floating gate dielectric") on the semiconductor substrate to separate the floating gate from the substrate, wherein the floating gate dielectric is made of the same material as the select gate dielectric but is thinner than the select gate dielectric.

23. (Original) The integrated circuit of Claim 18 further comprising a second peripheral transistor comprising a second peripheral transistor gate dielectric on the semiconductor substrate and a gate on the second peripheral transistor gate dielectric, wherein the second peripheral transistor gate dielectric is made of the same material as the select gate transistor gate dielectric and the first peripheral transistor gate dielectric but the thickness of the second peripheral transistor gate dielectric is different from the thickness of the first peripheral transistor gate dielectric.

24. (Original) The integrated circuit of Claim 23 wherein the second peripheral transistor gate dielectric is thinner than the first peripheral transistor gate dielectric.

25. (Original) The integrated circuit of Claim 23 wherein the select gate dielectric as at least as thick as a gate dielectric of any peripheral transistor in said memory.

26. (Original) The integrated circuit of Claim 18 wherein the memory cell is one of a plurality of nonvolatile memory cells of the integrated circuit, each memory cell comprising a dielectric ("select gate dielectric") on the semiconductor substrate, a select gate on the select gate dielectric, a floating gate, and a control gate;

wherein the select gate dielectric of each memory cell has the same thickness as the first peripheral transistor gate dielectric.

27. (Original) The integrated circuit of Claim 18 wherein during a memory cell writing operation, the first peripheral transistor is exposed to a voltage of a higher magnitude than any voltage provided to the memory cell in a reading operation.

28. (Original) The integrated circuit of Claim 27 wherein during the memory cell writing operation, the first peripheral transistor is exposed to a voltage of a higher magnitude than any power supply voltage provided to the nonvolatile memory.

29. (Original) The integrated circuit of Claim 18 wherein the memory cell is to support a writing operation in which the memory cell is written by a transfer of a charge between the floating gate and a channel region of the memory cell, the channel region being located in the semiconductor substrate.